National Semiconductor

LM20123
3A, 1.5MHz PowerWise® Synchronous Buck Regulator

General Description

The LM20123 is a full featured 1.5 MHz synchronous buck regulator capable of delivering up to 3A of continuous output current. The current mode control loop can be compensated to be stable with virtually any type of output capacitor. For most cases, compensating the device only requires two external components, providing maximum flexibility and ease of use. The device is optimized to work over the input voltage range of 2.95V to 5.5V making it suited for a wide variety of low voltage systems.

The device features internal over voltage protection (OVP) and over current protection (OCP) circuits for increased system reliability. A precision enable pin and integrated UVLO allows the turn on of the device to be tightly controlled and sequenced. Start-up inrush currents are limited by both an internally fixed and externally adjustable Soft-Start circuit. Fault detection and supply sequencing is possible with the integrated power good circuit.

The LM20123 is designed to work well in multi-rail power supply architectures. The output voltage of the device can be configured to track a higher voltage rail using the SS/TRK pin. If the output of the LM20123 is pre-biased at startup it will not sink current to pull the output low until the internal soft-start ramp exceeds the voltage at the feedback pin.

The LM20123 is offered in a 16-pin eTSSOP package with an exposed pad that can be soldered to the PCB, eliminating the need for bulky heatsinks.

Features

- Input voltage range 2.95V to 5.5V
- Accurate current limit minimizes inductor size
- 96% efficiency with 1.5 MHz switching frequency
- 32 mΩ integrated FET switches
- Starts up into pre-biased loads
- Output voltage tracking
- Peak current mode control
- Adjustable output voltage down to 0.8V
- Adjustable Soft-Start with external capacitor
- Precision enable pin with hysteresis
- Integrated OVP, UVLO, power good and thermal shutdown
- eTSSOP-16 exposed pad package
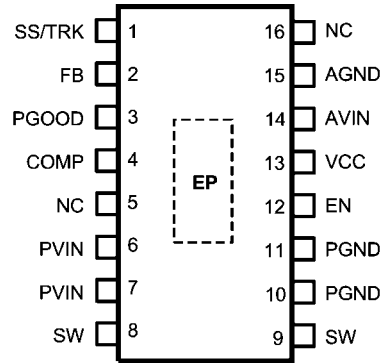
Applications

- Simple to design, high efficiency point of load regulation from a 5V or 3.3V bus
- High Performance DSPs, FPGAs, ASICs and microprocessors
- Broadband, Networking and Optical Communications Infrastructure

Typical Application Circuit
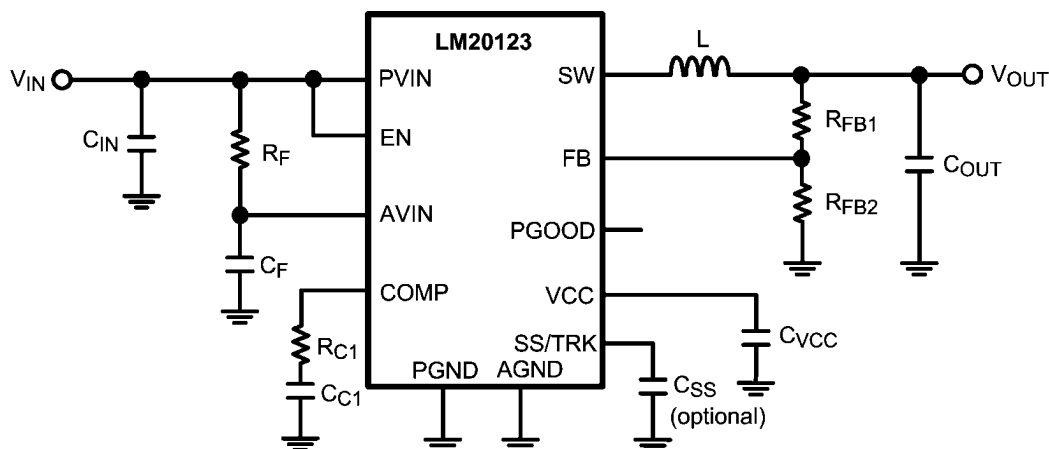
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Connection Diagram

Top View
eTSSOP-16 Package

30030102

Ordering Information

Order Number	Package Type	NSC Package Drawing	Package Marking	Supplied As
LM20123MH	eTSSOP-16	MXA16A	20123MH	92 Units of Rail
LM20123MHE				250 Units of Tape and Reel
LM20123MHX				2500 Units of Tape and Reel

Pin Descriptions

Pin #	Name	Description
1	SS/TRK	Soft-Start or Tracking control input. An internal 5 µA current source charges an external capacitor to set the Soft-Start ramp rate. If driven by a external source less than 800 mV, this pin overrides the internal reference that sets the output voltage. If left open, an internal 1ms Soft-Start ramp is activated.
2	FB	Feedback input to the error amplifier from the regulated output. This pin is connected to the inverting input of the internal transconductance error amplifier. An 800 mV reference connected to the non-inverting input of the error amplifier sets the closed loop regulation voltage at the FB pin.
3	PGOOD	Power good output signal. Open drain output indicating the output voltage is regulating within tolerance. A pull-up resistor of 10 kΩ to 100 kΩ is recommend for most applications.
4	COMP	External compensation pin. Connect a resistor and capacitor to this pin to compensate the device.
5,16	NC	These pins must be connected to GND to ensure proper operation.
6,7	PVIN	Input voltage to the power switches inside the device. These pins should be connected together at the device. A low ESR capacitor should be placed near these pins to stabilize the input voltage.
8,9	SW	Switch pin. The PWM output of the internal power switches.
10,11	PGND	Power ground pin for the internal power switches.
12	EN	Precision enable input for the device. An external voltage divider can be used to set the device turn-on threshold. If not used the EN pin should be connected to PVIN.
13	VCC	Internal 2.7V sub-regulator. This pin should be bypassed with a 1 µF ceramic capacitor.
14	AVIN	Analog input supply that generates the internal bias. Must be connected to VIN through a low pass RC filter.
15	AGND	Quiet analog ground for the internal bias circuitry.
EP	Exposed Pad	Exposed metal pad on the underside of the package with a weak electrical connection to ground. It is recommended to connect this pad to the PC board ground plane in order to improve heat dissipation.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltages from the indicated pins to GND

AVIN, PVIN, EN, PGOOD, SS/TRK, COMP, FB, SW	-0.3V to +6V
Storage Temperature	-65°C to 150°C
Junction Temperature	150°C

Power Dissipation (Note 2)	2.6W
Lead Temperature (Soldering, 10 sec)	260°C
Minimum ESD Rating (Note 3)	±2kV

Operating Ratings

PVIN, AVIN to GND	2.95V to 5.5V
Junction Temperature	−40°C to + 125°C

Electrical Characteristics

Unless otherwise stated, the following conditions apply: AVIN = PVIN = VIN = 5V. Limits in standard type are for T_J = 25°C only, limits in bold face type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{FB}	Feedback pin voltage	V_{IN} = 2.95V to 5.5V	**0.788**	0.8	**0.812**	V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	I_{OUT} = 100 mA to 3A		0.08		%/A
I_{CL}	Switch Current Limit Threshold	V_{IN} = 3.3V	**4.3**	4.8	**5.3**	A
R_{DS_ON}	High-Side Switch On Resistance	I_{SW} = 3.5A		36	**55**	mΩ
R_{DS_ON}	Low-Side Switch On Resistance	I_{SW} = 3.5A		32	**52**	mΩ
I_Q	Operating Quiescent Current	Non-switching, $V_{FB} = V_{COMP}$		3.5	**6**	mA
I_{SD}	Shutdown Quiescent current	V_{EN} = 0V		90	**180**	µA
V_{UVLO}	VIN Under Voltage Lockout	Rising V_{IN}	**2.45**	2.7	**2.95**	V
V_{UVLO_HYS}	VIN Under Voltage Lockout Hysteresis	Falling V_{IN}		45	**100**	mV
V_{VCC}	VCC Voltage	I_{VCC} = 0 µA	**2.45**	2.7	**2.95**	V
I_{SS}	Soft-Start Pin Source Current	$V_{SS/TRK}$ = 0V	**2**	4.5	**7**	µA
V_{TRACK}	SS/TRK Accuracy, V_{SS} - V_{FB}	$V_{SS/TRK}$ = 0.4V	**-10**	3	**15**	mV
Oscillator						
F_{OSC}	Oscillator Frequency		**1350**	1500	**1650**	kHz
DC_{MAX}	Maximum Duty Cycle	I_{LOAD} = 0A		85		%
T_{ON_TIME}	Minimum On Time			100		ns
T_{CL_BLANK}	Current Sense Blanking Time	After Rising V_{SW}		80		ns
Error Amplifier and Modulator						
I_{FB}	Feedback pin bias current	V_{FB} = 0.8V		1	**100**	nA
I_{COMP_SRC}	COMP Output Source Current	$V_{FB} = V_{COMP}$ = 0.6V	**80**	100		µA
I_{COMP_SNK}	COMP Output Sink Current	V_{FB} = 1.0V, V_{COMP} = 0.6V	**80**	100		µA
g_m	Error Amplifier Transconductance	I_{COMP} = ± 50 µA	**450**	510	**600**	µmho
A_{VOL}	Error Amplifier Voltage Gain			2000		V/V
Power Good						
V_{OVP}	Over Voltage Protection Rising Threshold	With respect to V_{FB}	**105**	108	**111**	%
V_{OVP_HYS}	Over Voltage Protection Hysteresis			2	**3**	%
V_{PGTH}	PGOOD Rising Threshold	With respect to V_{FB}	**92**	94	**96**	%
V_{PGHYS}	PGOOD Falling Hysteresis			2	**3**	%
T_{PGOOD}	PGOOD deglitch time			16		µs
I_{OL}	PGOOD Low Sink Current	V_{PGOOD} = 0.4V	**0.6**	1		mA
I_{OH}	PGOOD High Leakage Current	V_{PGOOD} = 5V		5	**100**	nA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Logic						
V_{IH_EN}	EN Pin Turn on Threshold	V_{EN} Rising	**1.08**	1.18	**1.28**	V
V_{EN_HYS}	EN Pin Hysteresis			66		mV
Thermal Shutdown						
T_{SD}	Thermal Shutdown			160		°C
T_{SD_HYS}	Thermal Shutdown Hysteresis			10		°C
Thermal Resistance						
θ_{JA}	Junction to Ambient			38		°C/W

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.
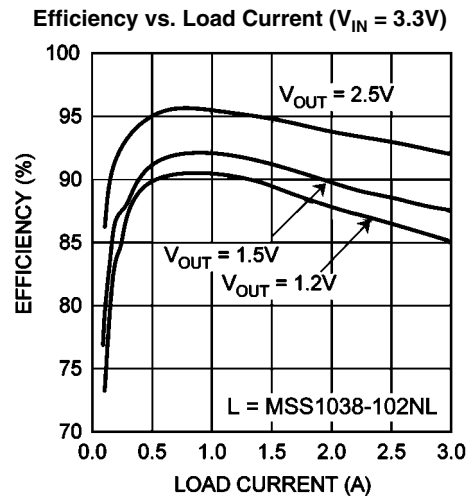
Note 2: The maximum allowable power dissipation is a function of the maximum junction temperature, T_{J_MAX}, the junctions-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{D\_MAX} = (T_{J\_MAX} - T_A)/\theta_{JA}$. The maximum power dissipations of 2.6W is determined using $T_A = 25°C$, $\theta_{JA} = 38°C/W$, and $T_{J\_MAX} = 125°C$.

Note 3: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor to each pin.

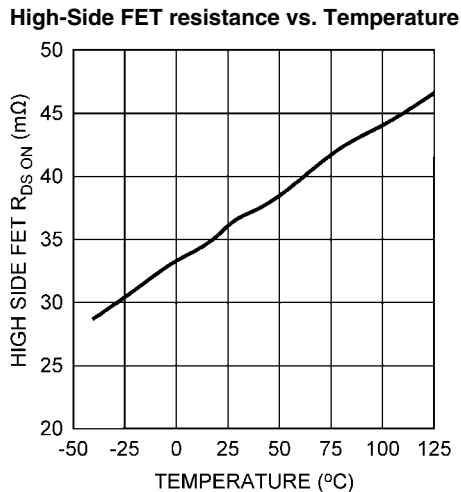## Typical Performance Characteristics

Unless otherwise specified: $C_{IN} = C_{OUT} = 100$ µF, L = 1.0 µH (Coilcraft MSS1038), $V_{IN} = 5V$, $V_{OUT} = 1.2V$, $R_{LOAD} = 1.2\Omega$, $T_A = 25°C$ for efficiency curves, loop gain plots and waveforms, and $T_J = 25°C$ for all others.

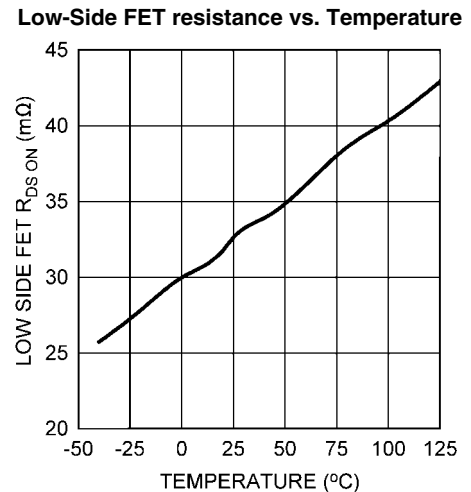**Efficiency vs. Load Current (V_{IN} = 5V)**

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Efficiency vs. Load Current (V_{IN} = 3.3V)

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High-Side FET resistance vs. Temperature

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Low-Side FET resistance vs. Temperature
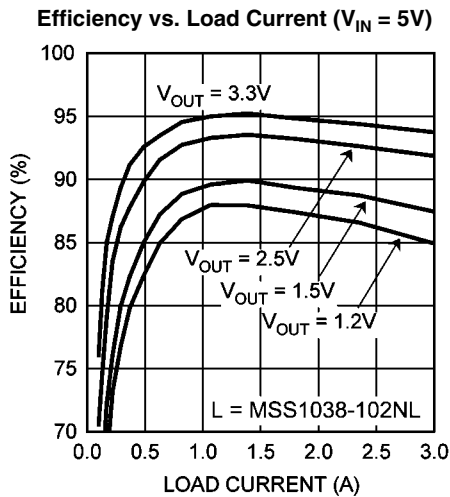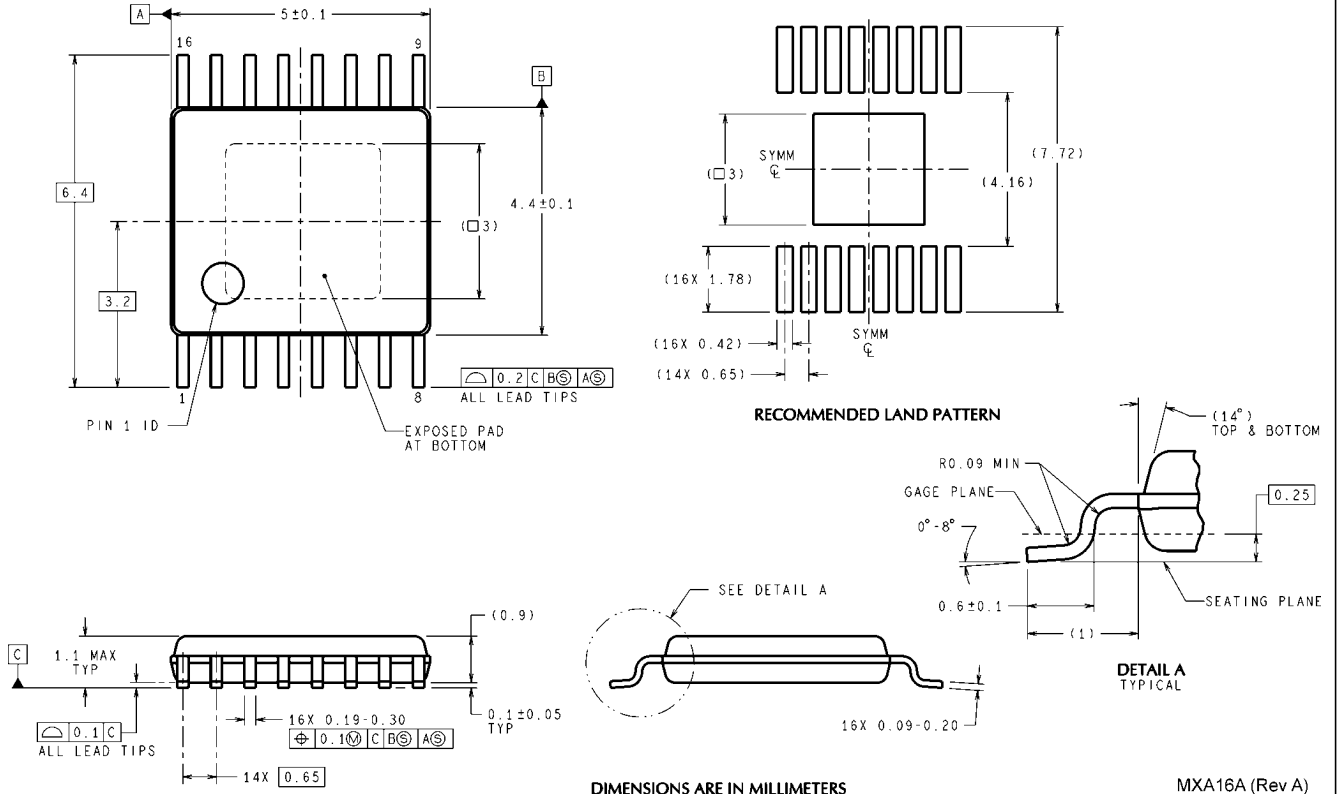

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Physical Dimensions inches (millimeters) unless otherwise noted

A ⊢— 5±0.1 —⊣

16   9

B

6.4

3.2

4.4±0.1

(□3)

1   8

⌒ 0.2 C B⑤ A⑤
ALL LEAD TIPS

PIN 1 ID

EXPOSED PAD
AT BOTTOM

RECOMMENDED LAND PATTERN

SYMM
Ȼ

(□3)

(7.72)

(4.16)

(16X 1.78)

(16X 0.42)

(14X 0.65)

SYMM
Ȼ

(14°)
TOP & BOTTOM

R0.09 MIN

GAGE PLANE

0°-8°

0.6±0.1

0.25

SEATING PLANE

(1)

DETAIL A
TYPICAL

C

1.1 MAX
TYP

(0.9)

0.1±0.05
TYP

⌒ 0.1 C
ALL LEAD TIPS

16X 0.19-0.30

⊕ 0.1Ⓜ C B⑤ A⑤

14X 0.65

SEE DETAIL A

16X 0.09-0.20

DIMENSIONS ARE IN MILLIMETERS
16-Lead eTSSOP Package
NS Package Number MXA16A

MXA16A (Rev A)